Leakage Power Reduction in Different Types of Full Adders Considering Delay-Power Tradeoff

Project Proposal, VLSI Design – ECE6332

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1. Introduction

With the advent of battery operated devices and scaling trends in deep submicron (DSM) regime, leakage power is becoming a large component for total power dissipation. High power consumption leads to reduction in the battery life in the case of battery-powered applications and effects reliability, packaging, and cooling cost. There are several different techniques for reducing leakage power. One is adding a sleep transistor between the pull-down-network and the ground to cutoff its connection to the ground when the circuit is in sleep mode. This technique is also called Power Gating. Another way for reducing leakage is stack forcing which uses the self-reverse bias effect when stack of transistors are turned OFF. In this research proposal, we want to explore delay-power tradeoff for different leakage power reduction techniques on different types of adders.

2. Research Problem

Full adders are important components in applications such as digital signal processors (DSP) architectures and microprocessors. Apart from the basic addition adders also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc. In most of these systems the adder lies in the critical path that determines the overall performance of the system. Furthermore, energy reduction of functional units is a very important concern for high-end superscalar processors. There are always tradeoff between power and delay. In this proposal, we want to consider different types of adders with different leakage power reduction techniques and try to figure out which combination of these two provide the best tradeoff for power and delay metrics.

3. Approach

We have started with three simple power gating techniques (Figure 1) on two types of adder, carry ripple adder and carry select adder with mirror topology. Using only headers or only footers or both have different impact on the power and delay trade off of the circuit. Appendix A shows the schematic and simulation (for outputs and power) for different techniques.

Table 1 and Table 2 present the average total power in the active mode and leakage power in the standby mode for one bit mirror topology full adder and one bit complementary full adder respectively. Three different power gating techniques have been applied to the adders and leakage power calculated for different inputs vectors to see the effect of the input in the leakage power in the standby mode.

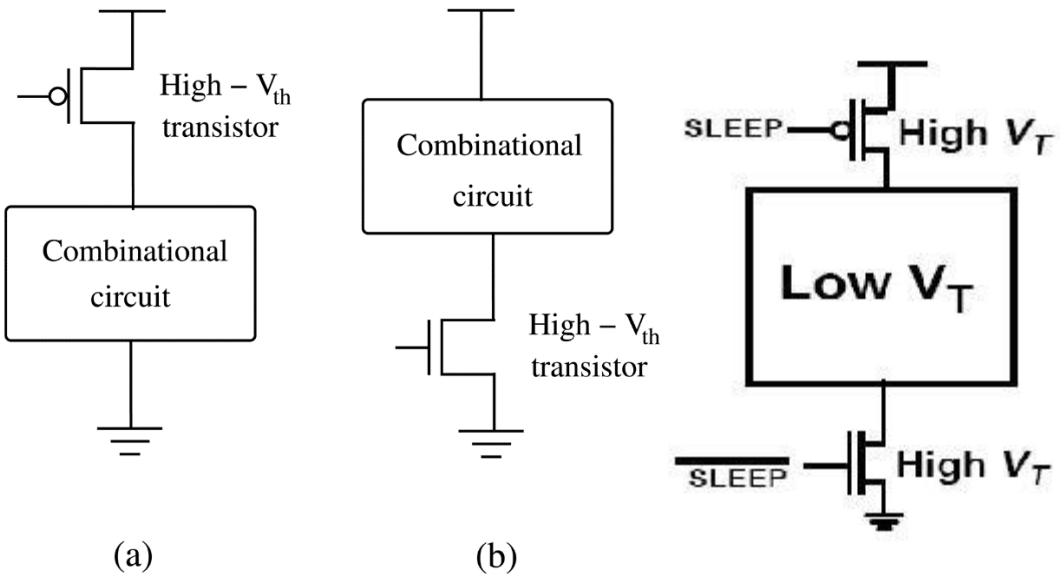

Figure1. Three power gating techniques: a. Header sleep transistor, b. Footer sleep transistor, c. Footer and header sleep transistors

Adder Type	Techniques	Total power in active mode (uW)	Leakage Power in Standby mode (nW) for different input vectors (ABCin)					Delay (ps)	
			000	010	101	111	avg	c	s
one bit mirror topology full adder	P.D.N. & P.U.N. sleepy transistors	59.77	77	102	109	67	88.75	49	81
	P.D.N. sleepy transistor	8.33	53	1290	562	107	503	37	59
	P.U.N. sleepy transistor	9.26	109	263	901	24	324.2	29	67

Table 1. Power and delay calculation for one bit mirror topology full adder

Adder Type	Techniques	Total power in active mode (uW)	Leakage Power in Standby mode (pW) for different input vectors (ABCin)					Delay (ps)	
			000	010	101	111	avg	c	s
one bit complementary full adder	P.D.N. & P.U.N. sleepy transistors	6.16	27	11	12	15	16.25	52	63
	P.D.N. sleepy transistor	6.15	1630	1440	811	31	978	37	59
	P.U.N. sleepy transistor	6.26	55	584	1170	1530	834.75	29	67

Table 2. Power and delay calculation for one bit complementary full adder

As it is shown in Table 1, for one bit mirror topology full adder, when we use a NMOS sleepy transistor in the P.D.N, the combination of inputs which are all zero give the lowest leakage power. On

the other hand, when we use PMOS sleepy transistor in the P.U.N, the combination of inputs which are all one gives the lowest leakage power. Although the average delay for the having both sleepy transistors in P.D.N and P.U.N give us the best average leakage power, but is has the largest delay. The lowest leakage power for the one bit mirror topology full adder accrues when there is a PMOS sleepy transistor in P.U.N and all of the inputs are one. It is just 7% of the average leakage power. It seems to be very promising to use a PMOS as a pass transistor to set all the inputs to one (sleep =1) in the standby mode. Figure 2 shows the design of one of the adder inputs. We need to calculate power and delay with the new designed circuit and see how much leakage power reduction has been gained and what its effect on delay is.

On the other hand, the results from one bit complementary full adder shows that when we use both header and footer sleep transistor, we have the lowest leakage power in compare to others. Even though the delay is more for this technique, but it seems to have best PDP when we use both footer and header sleep transistor in one bit complementary full adder.

As we understood from the simulation, each type of adder needs to have a special type of leakage reduction technique to present best PDP and it is not true to say that if one technique has the best PDP for adder type x, it has the best PDP for adder type y and they need different approach to take.

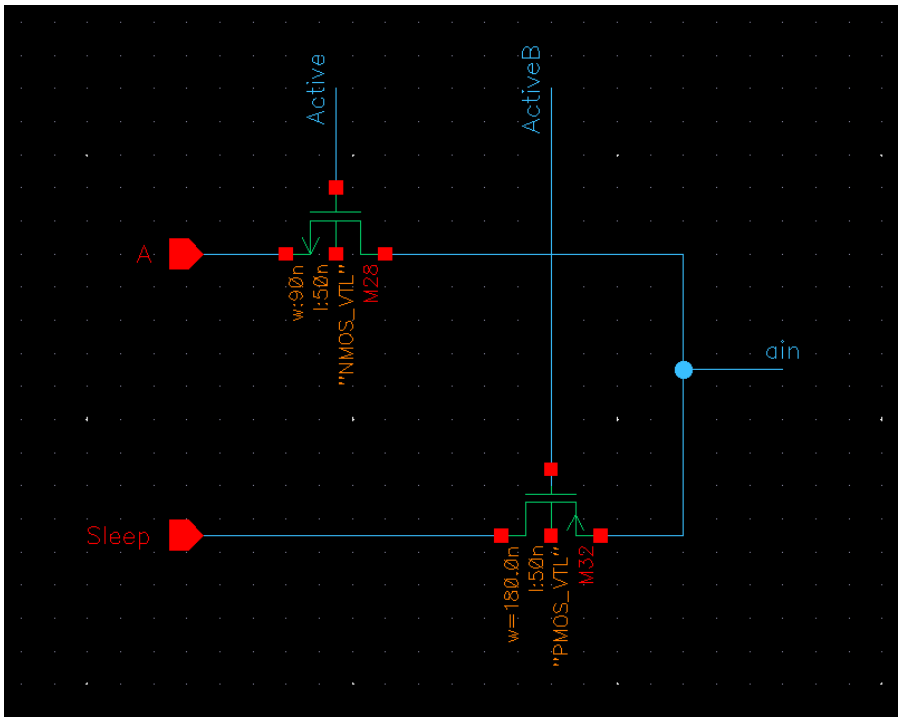

Figure2. Use sleep signal as a one bit mirror topology full adder inputs in standby mode and normal inputs in active mode

Not only different input vectors on different adders can have different effect on PDP, but also the size of sleep transistors play an important role in leakage power and delay.

4. Design

We have studied several leakage power reduction techniques [1-6] and we want to implement them first on different one bit adders like carry ripple adder, carry look ahead adder, and carry select adder. Then, we want to simulate these technique with 16 bit adders and figure out how it can present the best tradeoff for power and delay. There are three aspects we need to take:

- What is the best input vectors for each kind of adder
- Having separate sleep transistors for each single full adder and then, try to find the best approach for having shared sleep transistors for each kind of adder which leads to less PDP
- How we can improve power-delay tradeoff with changing sleep transistors size

5. Expected outcomes

By the end of this project, we expect to figure out that one specific approach which is the best for one kind of adder should not be necessarily the best approach for the other types of adders. Because different adders have different topologies. For example, if the adder topology is more close to mirror topology, we expect to have lowest PDP for certain input vectors (all zero or all one depends on the technique). And for the other topologies which are not close to mirror topology, it should not be true.

We expect to figure out which feature of the adders has effect on the approach we have to take to have the best PDP. Then, it gives us a general view and we can extent gained approach to the other types of logics.

6. Timeline

tasks	Weeks							
	8	9	10	11	12	13	14	15
Simulating 16 bit CSA with mirror topology and CRA and try to optimize PDP by taking mentioned approach	*							
Simulating other leakage reduction techniques on CSA mirror and CRA and take mentioned approach and try to achieve best PDP		*						
Simulating two other different adder with different techniques			*					
Analyzing the effect of sizing and sleep transistor sharing				*				
Preparing for design review 2					*			
Summaries and categorize the outcomes						*		
Write paper							*	
Write final report and prepare for the presentation								*

7. Task Breakdown

Task	who
Calculating power and delay for one bit mirror topology full adder mirror with proposed novelty	Elaheh
Simulating 16 bit CSA using one bit mirror topology full adder	Elaheh
Simulating 16 bit CRA using one bit complementary full adder	Luonan
Simulating 16 bit CLA	Luonan
Exploring best leakage power technique and PDP for each adder	Elaheh and Lounan
Exploring best possible inputs for having less leakage for each adder and each method	Elaheh and Lounan
A study on how to change transistor size to have better power delay performance	Elaheh and Lounan

8. References

[1] Rajani H.P., Srimannarayan Kulkarni, "NOVEL SLEEP TRANSISTOR TECHNIQUES FOR LOW LEAKAGE POWER PERIPHERAL CIRCUITS", International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.4, August 2012.

[2] Suhwan Kim ; Seoul Nat. Univ., Seoul ; Kosonocky, S.V. ; Knebel, D.R. ; Stawiasz, K., "A Multi-Mode Power Gating Structure for Low-Voltage Deep-Submicron CMOS ICs", IEEE Transactions, IEEE Circuits and Systems Society, Volume:54 , Issue: 7, July 2007.

[3] Kumar, Y., Paliwal, S. ; Rai, C.K. ; Balasubramanian, S.K., "A novel ground bounce reduction technique using four step power gating", Engineering and Systems (SCES), IEEE, 2013.

[4] Benton H. Calhoun, Frank A. Honoré, and Anantha P. Chandrakasan, "A Leakage Reduction Methodology for Distributed MTCMOS", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 39, NO. 5, MAY 2004.

[5] Anup Jalan and Mamta Khosla, "Analysis of Leakage Power Reduction Techniques in Digital Circuits", India Conference (INDICON), IEEE, 2011.

[6] Sathyabama University, Chennai, "Leakage Power Reduction in CMOS Modulo4 adder andModulo4 Multiplier in Sub-micron Technology", International Conference on Sustainable Energy and Intelligent System (SEISCON), 2011.

[7] http://venividiwiki.ee.virginia.edu/mediawiki/index.php/ToolsCadenceTutorialsBasic

[8] Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective", Second Editon, 2003.

Appendix A

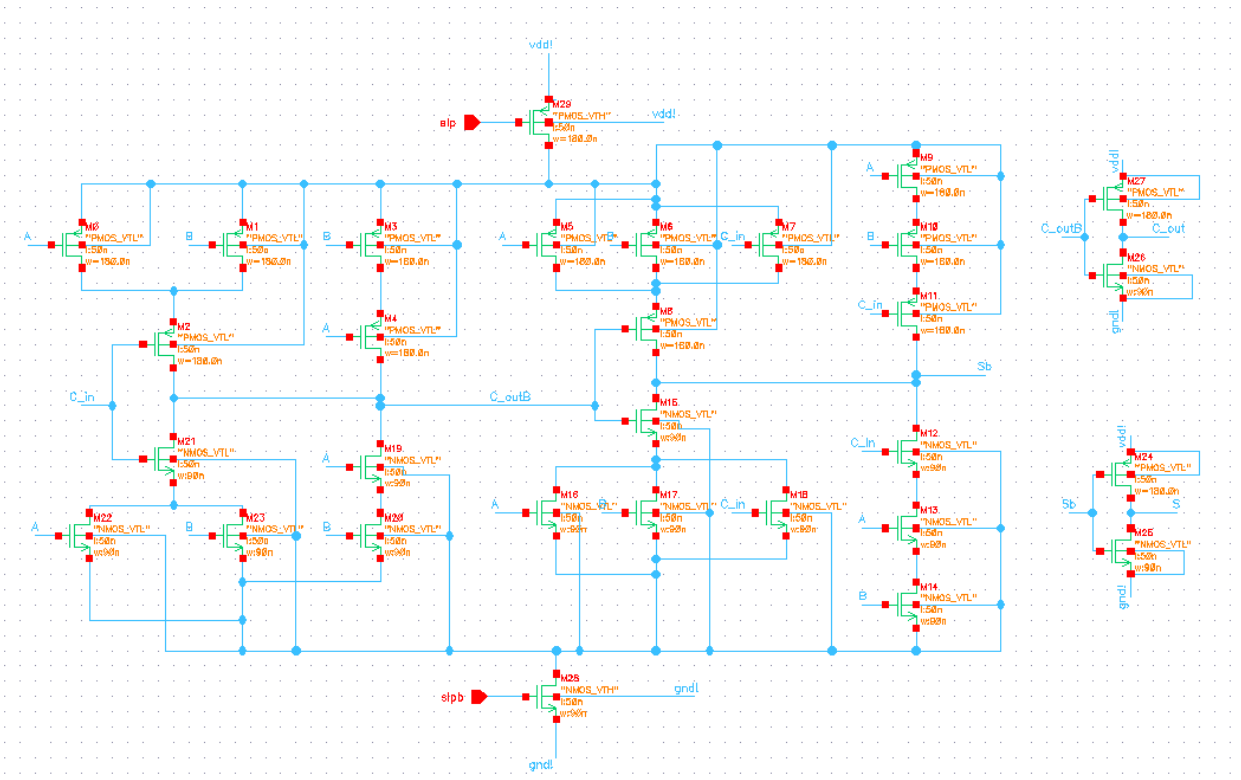

Figure 3. One bit mirror topology full adder with both footer and header sleep transistors

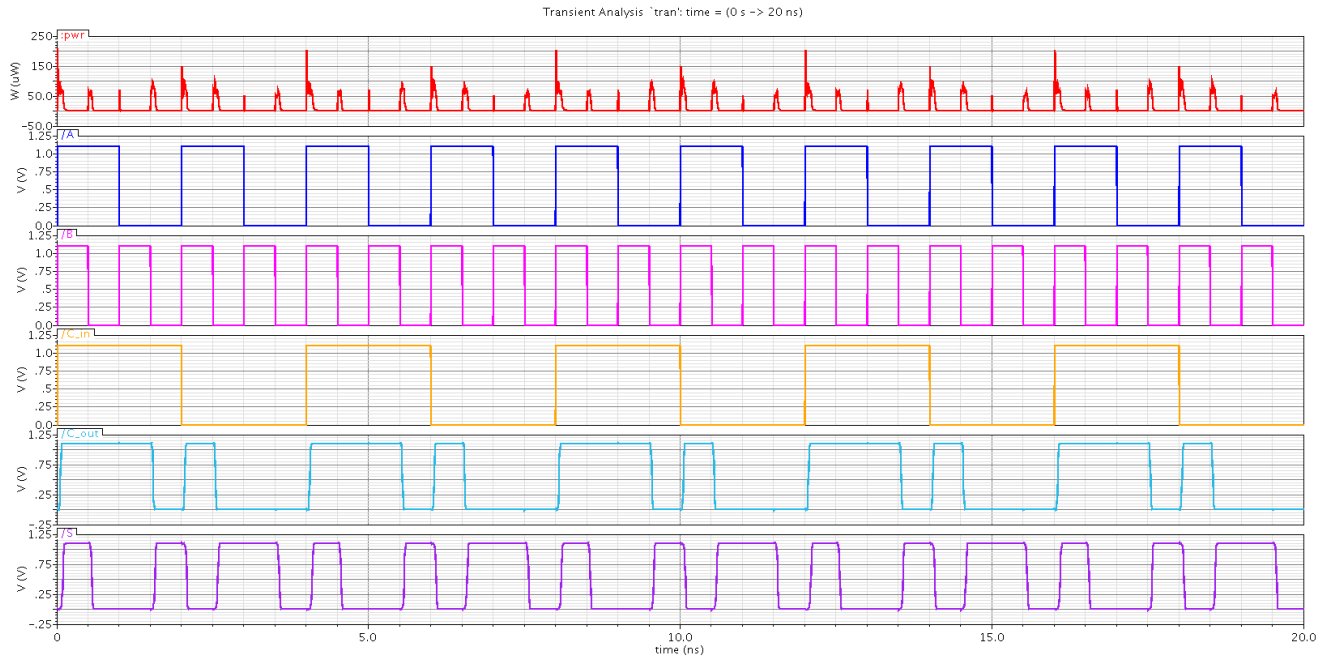

Figure 4. Simulation with total power curve in active mode for one bit mirror topology full adder and using both header and footer sleepy transistors

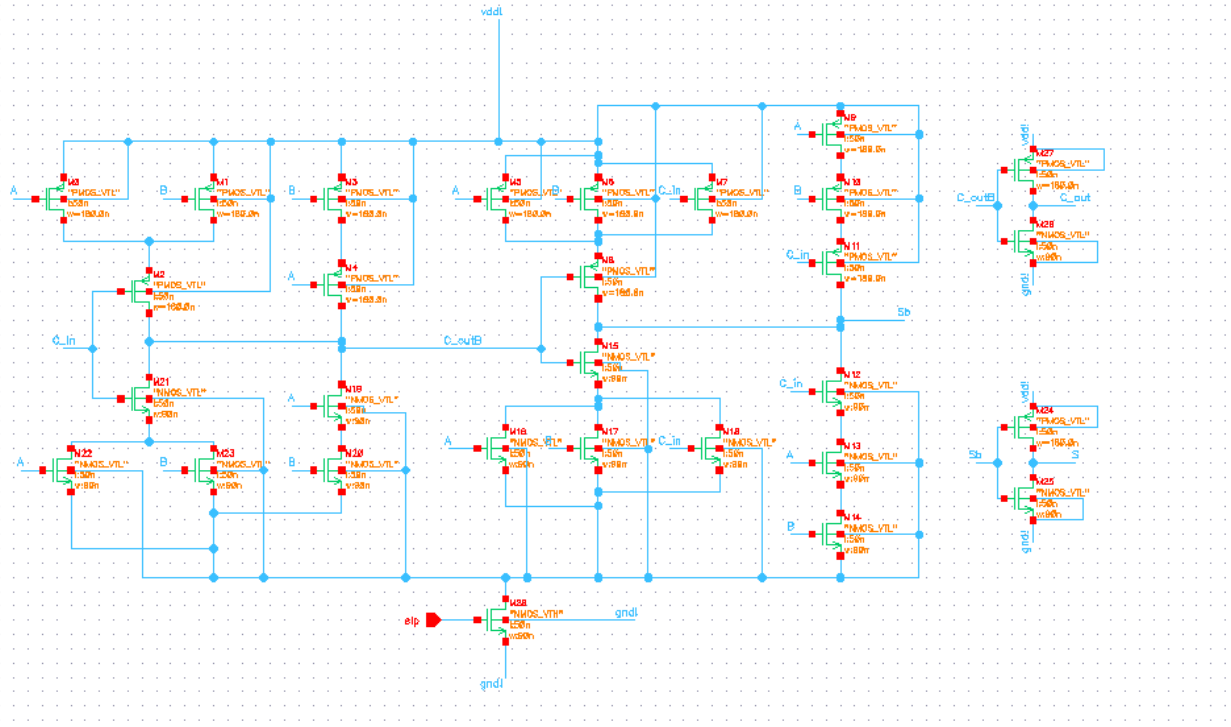

Figure 5. One bit mirror topology full adder with footer transistor

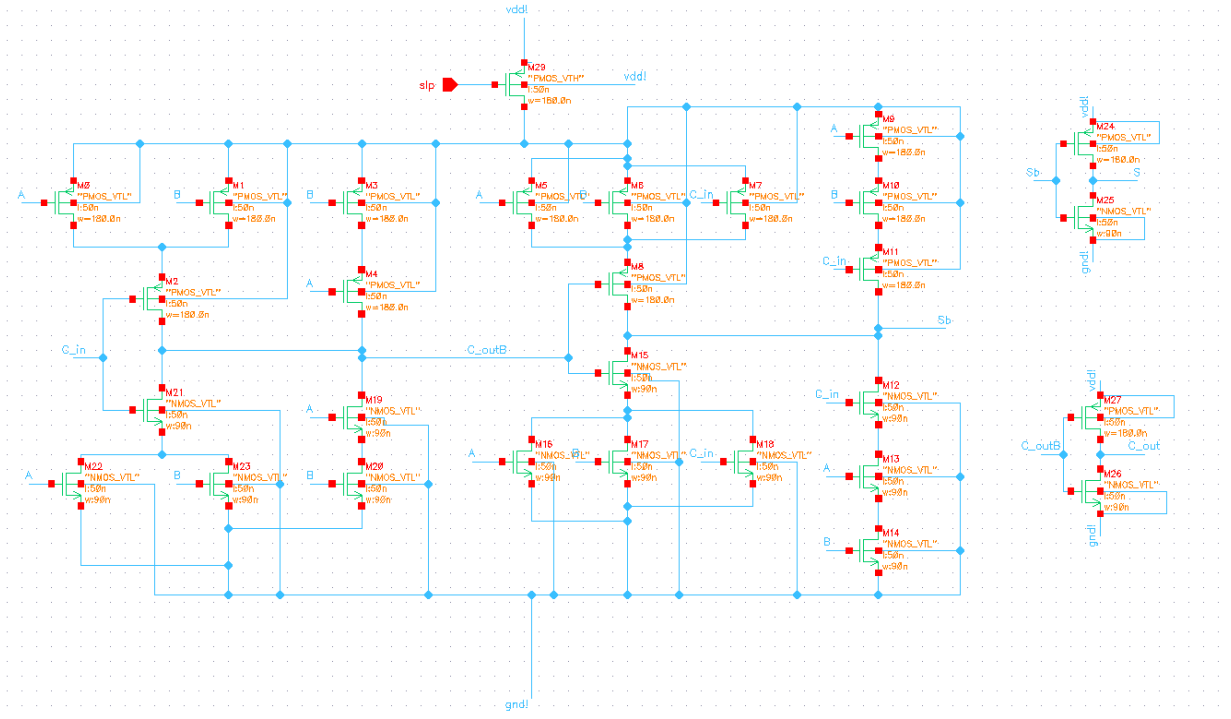

Figure 6. One bit mirror topology full adder with header transistor

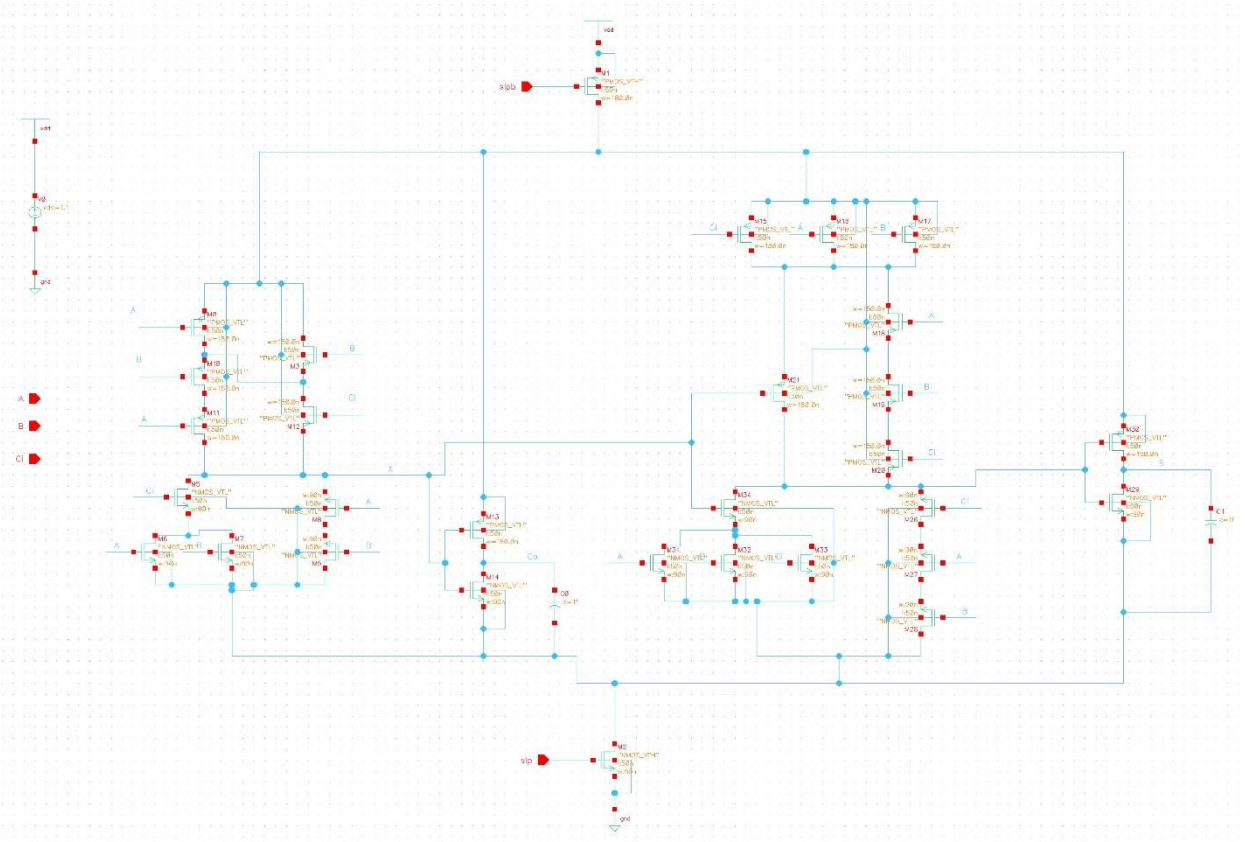

Figure7. One bit complementary full adder with both footer and header sleep transistors

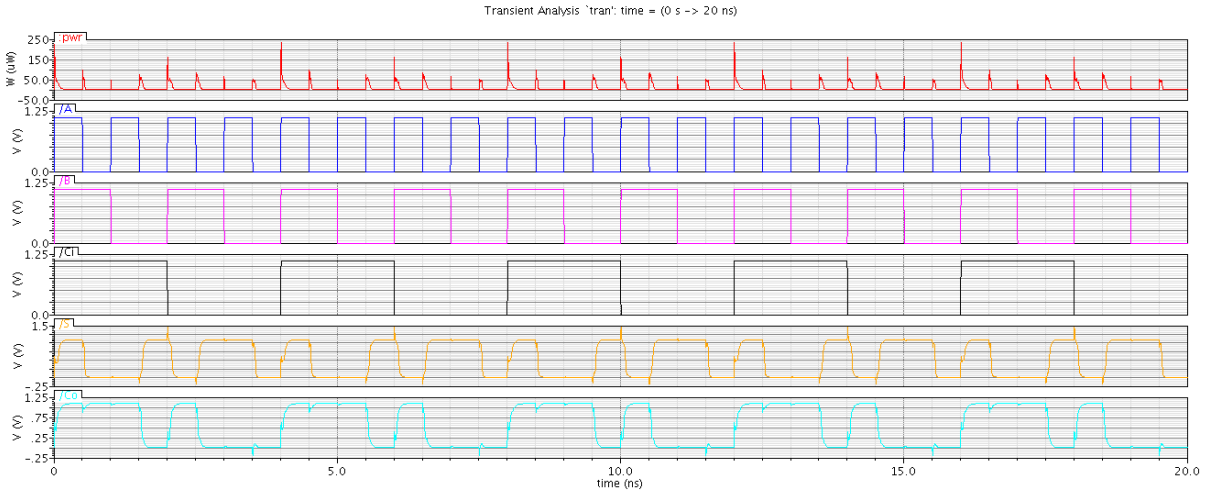

Figure 8. Simulation with total power curve in active mode for one bit complementary full adder and using both header and footer sleepy transistors

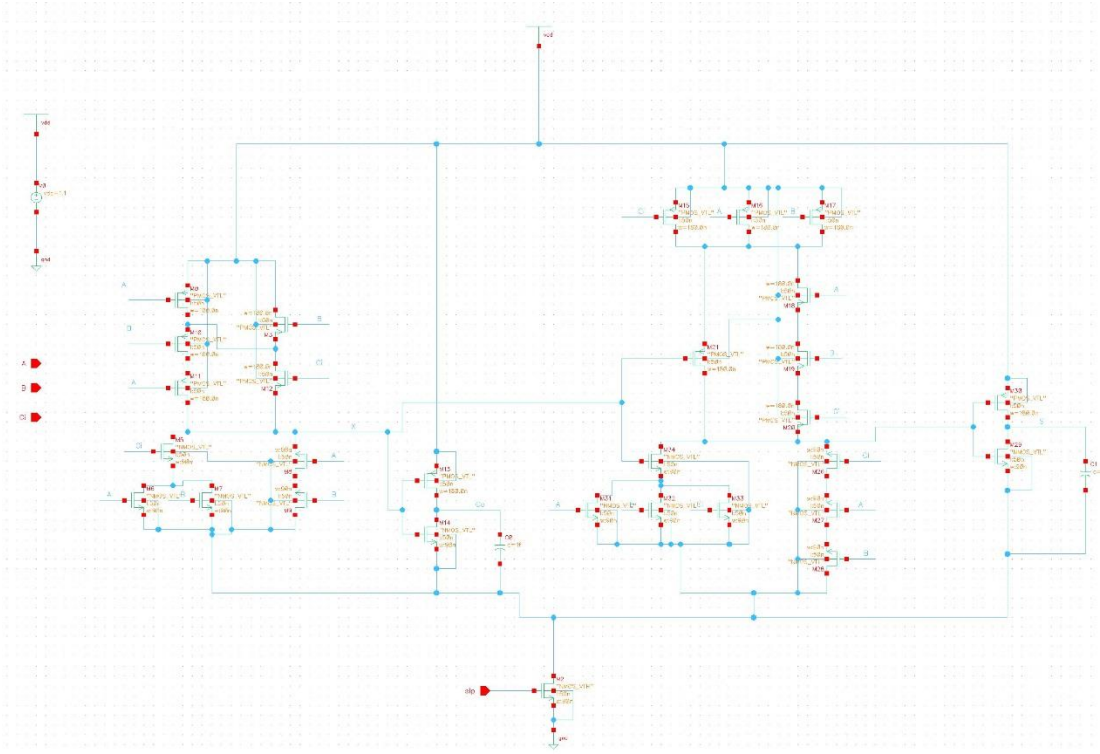

Figure 9. One bit complementary full adder with footer transistor

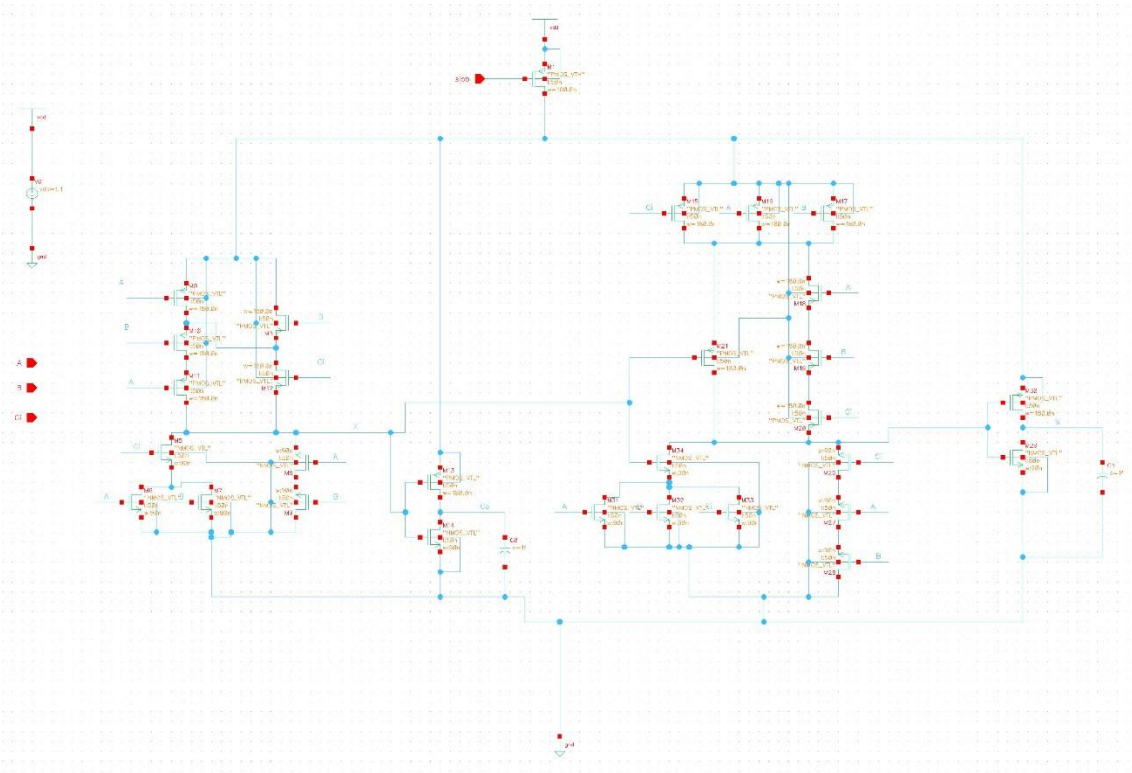

Figure 10. One bit complementary full adder with header transistor